10/083903

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Carl MIZUYABU, et al.

Assignee: ATI Technologies, Inc.

Title: SYSTEM FOR REDUCED POWER CONSUMPTION BY PHASE LOCKED LOOP AND METHOD THEREOF

Patent No.: 7,036,032 Issued: April 25, 2006

Atty. Docket No.: 1376-0200100

MS: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT—
PTO MISTAKE (37 C.F.R. § 1.322(a))**

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto, in duplicate, is Form PTO-1050, with at least one copy suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file: Response to Office Action dated November 11, 2005, pages 6 and 8
3. Please send the Certificate to:

J. GUSTAV LARSON
LARSON NEWMAN ABEL POLANSKY & WHITE, LLP
5914 WEST COURTYARD DRIVE, SUITE 200
AUSTIN, TEXAS 78730

Respectfully submitted,

6-16-06
Date

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PTO/SB/44 (05-03)
Approved for use through 01/31/2004. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,036,032

DATED : April 25, 2006

INVENTOR(S) : Carl Mizuyabu et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column No. 14, Line No. 27 change "looked" to –locked--

Column No. 15, Line No. 14 change "looked" to –locked--

MAILING ADDRESS OF SENDER:
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5914 West Courtyard Drive, Suite 200
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PATENT NO.: 7,036,032 B2

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MAY 09 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Carl MIZUYABU et al.		
Title:	SYSTEM FOR REDUCED POWER CONSUMPTION BY PHASE LOCKED LOOP AND METHOD THEREOF		
App. No.:	10/083,903	Filed:	02/27/2002
Examiner:	PATEL, Nitin C.	Group Art Unit:	2116
Customer No.:	34456	Confirmation No.:	4958
Atty. Dkt. No.:	1376-0200100		

Mail Stop AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed September 7, 2005, please amend the above-identified application as follows:

Claim Amendments begin on page 2.

Remarks begin on page 9.

CERTIFICATE OF TRANSMISSION/MAILING
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 6/22/06.

Judy Carey
Typed or Printed Name

Signature

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method comprising:
determining a power mode for a device;
disabling a phase locked loop by reducing power used for driving the phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode; and
providing the oscillator signal to an input of the phase locked loop and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

2. (Original) The method as in Claim 1, wherein the device consumes less power in the first power mode than in the second power mode.

3. (Previously Presented) The method as in Claim 1, further including suspending processing within the device when in a third power mode.

4. (Currently Amended) The method as in Claim 1, wherein the oscillator signal is generated through a crystal oscillator.

5. (Original) The method as in Claim 1, wherein the oscillator signal is generated through an RC circuit.

6. (Original) The method as in Claim 1, wherein the output of the phase locked loop is coupled to a clock divider and an output associated with the clock divider is coupled to the clock line.

7. (Previously Presented) The method as in Claim 6, wherein:

disabling the phase locked loop, when in the first power mode, includes providing the oscillator signal to the input of the clock divider; and

providing the oscillator signal to the phase locked loop, when in the second power mode, includes providing the locked signal to the input of the clock divider.

8. (Previously Presented) The method as in Claim 1, wherein disabling the phase locked loop, when in the first power mode, further includes providing reduced power, in comparison to an available power, to the device.

9. (Previously Presented) The method as in Claim 1, wherein disabling the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

10. (Canceled)

11. (Canceled)

12. (Previously Presented) The method as in Claim 9, wherein providing the oscillator signal to the phase locked loop, when in the second power mode, further includes using the maximum number of bits used to represent multimedia data.

13. (Original) The method as in Claim 1, wherein the device includes a portable device.

14. (Original) The method as in Claim 13, wherein the portable device includes a personal digital assistant.

15. (Previously Presented) The method as in Claim 1, wherein providing the oscillator signal to the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

16. (Original) The method as in Claim 15, wherein multimedia data includes video data.

17. (Original) The method as in Claim 15, wherein multimedia data includes audio data.

18. (Previously Presented) The method as in Claim 15, wherein disabling the phase locked loop, when in the first power mode, further includes using the maximum number of bits used to represent the multimedia data.

19. (Original) The method as in Claim 1, wherein disabling the phase locked loop includes shutting off power used for driving the phase locked loop.

20. (Currently Amended) The method as in Claim 1, wherein providing the oscillator signal to drive a clock line includes coupling a line carrying the oscillator signal to the clock line and wherein providing the locked signal from an output of the phase locked loop to the clock line includes decoupling the line carrying the oscillator signal from the clock line.

21. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying a number of pending instructions.

22. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying types of pending applications.

23. (Previously Presented) The method as in Claim 1, wherein determining the power mode includes identifying a change in display content.

24. – 35. (Canceled)

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36. (Currently Amended) A computer readable medium tangibly embodying a program of instructions to manipulate a system to:

determine a power mode for the system;

disable a phase locked loop by shutting of power used for driving the phase locked loop and ~~providing~~ provide an oscillator signal to drive a clock line when in a first power mode; and

provide the oscillator signal to an input of the phase locked loop and ~~providing~~ provide a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

37. (Original) The computer readable medium as in Claim 36, wherein the system consumes less power in the first power mode than in the second power mode.

38. (Previously Presented) The computer readable medium as in Claim 36, wherein the program of instructions is further used to:

represent multimedia data using a first number of bits when in the first power mode; and

represent multimedia data using a second number of bits when in the second power mode, wherein the first number of bits are less than the second number of bits.

39. (Original) The computer readable medium as in Claim 38, wherein the multimedia data includes video data.

40. (Original) The computer readable medium as in Claim 38, wherein the multimedia data includes audio data.

41. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a number of pending instructions.

42. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a change in display content.

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43. (Original) The computer readable medium as in Claim 36, wherein the power mode determined is based on a type of instructions stored in the instruction buffer.

44. (Previously Presented) A system comprising:

a phase locked loop having a first input to receive a first clock signal and a first output to provide a second clock signal, wherein the second clock signal is based on the first clock signal;

a first multiplexer having a first input coupled to the first input of the phase locked loop, a second input coupled to the first output of the phase locked loop and an output, wherein the first multiplexer is operable to selectively provide to the output a signal received at the first input when in a first power mode or a signal received at the second input when in a second power mode; and

means for disabling the phase locked loop by reducing power used for driving the phase locked loop when in the first power mode.

45. (Previously Presented) The system as in Claim 44, further comprising:

a first clock divider having an input coupled to the output of the first multiplexer and an output coupled to a first bus.

46. (Previously Presented) The system as in Claim 45, further comprising:

a second multiplexer having a first input coupled to the first input of the phase locked loop, a second input coupled to the first output of the phase locked loop and an output, wherein the second multiplexer is operable to selectively provide to the output a signal received at the first input when in the first power mode or a signal received at the second input when in the second power mode; and

a second clock divider having an input coupled to the output of the second multiplexer and an output coupled to a second bus.

47. (Previously Presented) The system as in Claim 44, further comprising:
means for determining a power mode of the system; and
means for providing a control signal to the first multiplexer based on the determined power mode.

48. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a number of pending instructions.

49. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a type of pending instruction.

50. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a rate of change in a number of pending instructions.

51. (Previously Presented) The system as in Claim 47, wherein the means for determining a power mode of the system includes means for determining a change in display content.

52. (Previously Presented) The system as in Claim 44, wherein the means for disabling the phase locked loop includes means for shutting off a supply of power to the phase locked loop.

53. (Previously Presented) The system as in Claim 44, further comprising:
an oscillator having an output coupled to the first input of the phase locked loop, wherein the oscillator is operable to output the first clock signal.

54. (Previously Presented) The system as in Claim 53, further comprising means for disabling an output of the first clock signal by the oscillator when in the first power mode.

55. (New) The method as in Claim 1, wherein:

providing the oscillator signal to drive the clock line includes providing the oscillator signal ~~to the clock~~ line via a first input of a multiplexer; and

providing the locked signal from the output of the phase locked loop to the clock line includes providing the locked signal to the clock line via a second input of the multiplexer.

56. (New) The computer readable medium as in Claim 36, wherein:

providing the oscillator signal to drive the clock line includes providing the oscillator signal to the clock line via a first input of a multiplexer; and

providing the locked signal from the output of the phase locked loop to the clock line includes providing the locked signal to the clock line via a second input of the multiplexer.

REMARKS

The Office Action dated September 7, 2005 has been received and carefully considered. In this response, claims 4, 20 and 36 have been amended, claims 10 and 11 have been canceled without prejudice and new claims 55 and 56 have been added. The amendments to claims 4 and 36 correct various informalities and do not narrow the scope of the claims. Support for the amendments and the addition of the new claims may be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claim 50

The Applicants note with appreciation the indication at page 19 of the Office Action that claim 50 would be allowable if rewritten in independent form. The Applicants have elected to forgo rewriting claim 50 as suggested in view of the following remarks.

Anticipation Rejection of Claims 1-8, 13, 14, 19, 20, 36 and 37

At page 2 of the Office Action, claims 1-8, 13, 14, 19, 20, 36 and 37 were rejected under 35 U.S.C. Section 102(b) as being anticipated by Challen (U.S. Patent No. 4,521,918). This rejection is respectfully traversed for at least the reason that Challen fails to disclose the particular combinations of features recited by these claims.

To illustrate, claim 1, from which claims 2-8, 13, 14, 19 and 20 depend, recites the features of providing an oscillator signal to drive a clock line and providing a locked signal from an output of a phase locked loop to the clock line. Claim 36 recites similar features vis-à-vis a clock line. Challen, however, fails to disclose clock signaling or a clock line in any manner, much less that an oscillator signal is used to drive a clock line or that a locked signal from an output of a phased locked loop is provided to a clock line as provided by claims 1 and 36. Rather, Challen discloses that its system is used as a frequency synthesizer for use in radio frequency (RF) transmissions, such as cellular telephone transmissions. *See, e.g., Challen*, Abstract; *see also Challen*, Fig. 2. One of ordinary skill in the art will appreciate that the signal line contemplated by Challen is not the same as, or even analogous to, a clock line as provided

by claims 1 and 36. Accordingly, Challen fails to disclose or even suggest each and every feature of claims 1 and 36, as well as the additional features of claims 2-8, 13, 14, 19, 20 and 37 at least by virtue of their dependency from one of claims 1 or 36. Moreover, these claims recite additional, non-obvious features.

To illustrate, claim 4 recites the features of wherein the oscillator signal is generated through a crystal oscillator and claim 5 recites the features that the oscillator signal is generated through an RC circuit. The Office Action asserts that the passage of Challen at col. 1, lines 9-16 disclose these features. *Office Action*, p. 3. However, this cited passage of Challen fails to disclose the generation of an oscillator signal through an RC circuit in any manner and therefore fails to disclose the additional features of claim 5. With respect to the features of claim 4, the disclosed system of Challen is a high frequency synthesizer and the cited passage of Challen discloses that "[h]igh frequency synthesizers [such as the one disclosed by Challen] are now commonly utilized *substitutes for the crystal controlled transmitter oscillators and receiver local oscillators* because they are able to provide a frequency stable signal at any one of a plurality of frequencies without the need for a crystal for each frequency." *Challen*, col. 1, lines 9-16 (emphasis added). Thus, Challen explicitly teaches that its frequency synthesizer is a substitute for (and therefore does not utilize) crystal controlled transmitter oscillators.

As another example, claim 8 recites the features of wherein disabling the phase locked loop, when in the first power mode, further includes providing *reduced* power, in comparison to an available power, to the device. The Office appears to erroneously interpret the provision of *reduced* power to include the provision of *no* power. However, one of ordinary skill in the art would understand that the provision of reduced power, in comparison to an available power, as provided by claim 8 does not include providing *no* power. Thus, as Challen discloses that power is either supplied to the PLL means 10 or is entirely shut-off, Challen fails to disclose providing *reduced* power, in comparison to an available power, as recited by claim 8.

As another example, claim 20 has been amended to recite the features of wherein providing the oscillator signal to drive a clock line includes coupling a line carrying the oscillator signal to the clock line and wherein providing the locked signal from an output of the phase locked loop to the clock line includes decoupling the line carrying the oscillator signal from the

clock line. As taught by Challen, the output of the VCO 12 is always coupled to the "output" and the line carrying the output of the VCO 12 is not decoupled at any time.

In view of the foregoing, it is respectfully submitted that the Office Action fails to establish that Challen discloses each and every feature recited by claims 1 and 36, as well as the additional features recited by dependent claims 2-8, 13, 14, 19, 20 and 37. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 1-8, 13, 14, 19, 20, 36 and 37 is respectfully requested.

Obviousness Rejection of Claims 44, 45, 47, 48 and 52-54

At page 5 of the Office Action, claims 44, 45, 47, 48 and 52-54 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov (U.S. Patent No. 6,691,215) and further in view of Challen. This rejection is respectfully traversed for at least the reason that there is no motivation to combine the teachings of Mirov and Challen as proposed.

The Office Action proposes the combination of Mirov and Challen to arrive at the particular combinations of features recited by claims 44, 45, 47, 48 and 52-54. The alleged rationale for this proposed combination is that "it would have been obvious . . . to modify the disabling of [the] PLL disclosed by Mirov to include removing power during [a] battery save operation . . . as taught by Challen, in order to obtain [a] frequency synthesizer without substantial drift [and which] can be reclocked in short [a] short period of time." *Office Action*, p. 6. As a first issue, the system of Challen is an analog system that provides an analog signal for use in an RF or analog cellular system, whereas Mirov is a digital system used to synchronize to a clock signal. Thus, not only are Challen and Mirov non-analogous art, their differing signaling modes prevents the efficient integration of one system into the other without considerable design effort. As a second issue, there is no motivation in either Mirov or Challen for their combination. Contrary to the assertions of the Office Action, Mirov provides no suggestion that it seeks to "a frequency synthesizer without substantial drift" as the system of Mirov is described in the context of a memory system (see Mirov, Abstract) and Mirov fails to suggest its use in an RF system or other analog system in which a frequency synthesizer would be useful. Likewise, Challen provides no suggestion that it seeks to synchronize clock signals and therefore fails to

suggest its use in a memory system or other digital system in which clock synchronization would be useful.

Accordingly, as one of ordinary skill in the art would have great difficulty integrating the analog system of Challen with the digital system of Mirov, and as neither Challen nor Mirov provide any motivation for such integration, one of ordinary skill in the art would find no motivation to combine the teachings of Mirov and Challen as proposed by the Office Action. The Office Action therefore fails to establish a *prima facie* case of obviousness of claims 44, 45, 47, 48 and 52-54. Moreover, these claims recite non-obvious features.

To illustrate, claim 48 recites the features of wherein the means for determining a power mode of the system includes means for determining a number of pending instructions. The Office Action asserts that the passages at col. 4, lines 4 and 31-50, col. 6, lines 49-67, col. 7, lines 1-24, and col. 17, lines 26-41 disclose the claimed features. However, as acknowledged at page 10 of the Office Action, neither the cited passages nor any other passages of Mirov disclose or even suggest a means for determining a number of pending instructions, much less that these means are included in the means for determining a power mode of the system as recited by claim 48.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 44, 45, 47, 48 and 52-54 is improper at this time. Reconsideration and withdrawal of this obviousness rejection therefore is respectfully requested.

Obviousness Rejections of Claims 9-12, 14-18, 21-23, 38-43, 46, 48, 49 and 51

At page 7 of the Office Action, claim 46 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov and Challen and further in view of Zhang (U.S. Patent No 6,687,322). At page 9 of the Office Action, claims 48 an 49 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov and Challen and further in view of Durham (U.S. Patent No 6,785,829). At page 11 of the Office Action, claim 51 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov and Challen and further in view of Anwyl (U.S. Patent No 5,576,738). At page 13 of the Office Action, claim 14 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Challen and claims 21, 22, 41 and 43

were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Challen and further in view of Durham. At page 15 of the Office Action, claims 23 and 42 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Challen and further in view of Anwyl.[1] At page 16 of the Office Action, claims 9-12, 15-18 and 38-40 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Challen and further in view of Zhang. These rejections are respectfully traversed.

Claims 9, 12, 14-18 and 21-23 depend from claim 1 and claims 38-43 depend from claim 36. As discussed above, Challen fails to disclose or even suggest each and every feature recited by claims 1 and 36. The Office Action does not assert that Mirov, Durham, Anwyl or Zhang disclose or suggest the features of claims 1 and 36 lacking in Challen, nor in fact are these features disclosed by the remaining cited references. Accordingly, the proposed combinations of Challen, Durham, Anwyl and Zhang fail to disclose or suggest the features of claims 9, 12, 14-18, 21-23 and 38-43 at least by virtue of their dependency from one of claims 1 or 36. Moreover, these claims recite additional non-obvious features.

Claims 46, 48, 49 and 51 depend from claim 44. As discussed above with respect to claim 44, there is no motivation to combine the teachings of Challen and Mirov as proposed by the Office Action. Moreover, the teachings of Durham, Anwyl and Zhang fail to provide the necessary motivation. Accordingly, the Office Action fails to establish a *prima facie* case of obviousness for claims 46, 48, 49 and 51 at least by virtue of their dependency from claim 44. Moreover, these claims recite additional non-obvious features.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 9, 12, 14-18, 21-23, 38-43, 46, 48, 49 and 51 are improper at this time. Reconsideration and withdrawal of these obviousness rejections therefore is respectfully requested.

Addition of New Claims 55 and 56

New claims 55 and 56 have been added. New claim 55 depends from claim 1 and recites the additional features of providing the oscillator signal to drive the clock line includes providing the oscillator signal to the clock line via a first input of a multiplexer and providing the locked

[1] The Office Action mistakenly identifies Challen as "Challenge" at pages 15 and 16 of the Office Action.

signal from the output of the phase locked loop to the clock line includes providing the locked signal to the clock line via a second input of the multiplexer. Claim 56 depends from claim 36 and recites similar features. It is respectfully submitted that the cited references fail to disclose or suggest, individually or in combination, these recited features.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

11 November 2005
Date

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